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IMPLEMENTATION OF POWER EFFICIENT PROGRAMMABLE PRPG USING BS-LFSR BASED ON BIST

S . Sajida*, C . Ravi Shankar Reddy

[*] PG Scholar, Dept. of ECE, JNTUCEA, Anantapur, Andhra Pradesh, India
Lecturer, Dept. of ECE, JNTUCEA, Anantapur, Andhra Pradesh, India

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ABSTRACT

This paper describes a low-power programmable generator with bit swapping technique which is capable of producing pseudorandom test patterns with toggle selection(TOSE) , enhanced fault coverage and power optimization compared to present BIST with normal LFSR based Pseudorandom pattern generator. It consists of a BS-LFSR driving a phase shifter with features like producing binary sequences with TOSE activity. A method is introduced to automatically select different controls of the generator for easy and precise tuning. Same technique is used to deterministically guide the generator towards test sequences with improved fault coverage to pattern count ratio. This paper proposes a LP test compression method that allows the power envelope to be predictable, flexible and accurate using TOSE based LBIST. The proposed hybrid scheme efficiently combines test compression with LBIST, where both techniques work to deliver high quality test.

KEYWORDS: Linear feedback shift register (LFSR), Built-in-self-test (BIST), low-power (LP) test,Toggle selection(TOSE).

INTRODUCTION

Today's electronics revolution is driven by market demands to provide better, cheaper, smaller and faster products while meeting users quality demands. Meeting these quality requirements necessitates performing adequate test and diagnosis procedures. Ensuring reliable and high quality microelectronics products has always been the primary objective of semiconductor test from years. However, conditions and the corresponding solutions undergo a significant evolution characterized by next technology nodes for example 3-D, design characteristics, and design processes, to name just a few key factors. New types of defects and patterns inevitably raise the questions of how sustainable the current test schemes are and what matching design-for-test (DFT) methods may soon be needed. For example, it is not clear whether test data compression the very successful and industry-proven DFT methodology of the last decade will be capable to encounter through the rapid rate of technological changes and the resultant test challenges. In recent times, logic built-in self-test (LBIST) is in use with test compression which was developed for system, board and infield test. This hybrid approach allows LBIST to combat with the best manufacturing test techniques by providing the abilities to run at-speed power aware tests and to reduce the test cost while preserving or augmenting all LBIST and scan compression advantages.

LITERATURE SURVEY

LBIST and test compression together has been made a vital research and development area to overcome the obstruction of test data bandwidth between tester and the chip. Other hybrid BIST schemes store deterministic patterns used to detect faults in a compressed form and use hardware to decompress them. In the paper [3], it is stated that as LBIT alone is not sufficient for the fault coverage an additional top up of deterministic test patterns are added for external tester. The combination of LBIST and deterministic ATPG is addressed which forms hybrid test patterns. These patterns can be generated using STUMPS architecture. They reduce external data tester memory and also number of pseudorandom patterns. But it has huge hardware circuitry for that consumes more area. This method also needs initial pattern storage which might not be efficient in general cases.

An ATPG to minimize ATE storage requirements and bandwidth between in [4][12]. Dynamic Compaction and allowing constraints on inputs of circuits can achieve tailored deterministic test patterns.A partially rotational scan

register is used in [5] for the n-detection of BIST so that unmodeled faults are detected. For selecting test patterns from ATPG a procedure is presented which reduces number of input vectors from external tester.

New programmable deterministic BIST method is developed to lower storage of deterministic patterns than previous methods and increase flexibility of internal and external test. In LFSR seed more care bits can be encoded as the information is stored using compression and decompression in memory as in [6].

LFSR reseeding is an effective methodology for lessening test storage. The encoding plan in [7] gives an approach to diminish the test power for LFSR[11] reseeding while as yet protecting or notwithstanding enhancing the pressure that is accomplished. The square size can be effectively conformed to tradeoff test-power lessening versus equipment overhead. The proposed plan can be utilized as a part of either a BIST situation or in test pressure plans in view of LFSR reseeding to fulfill power imperatives.

Due to high data switching in scan based test may consume more power. Full toggle scan patterns might also draw more power over mission mode. High power consumption may result in voltage noise, power droop or excessive peak power over multiple cycles which inturn leads to device damage, reduced chip reliability, short product lifetime or malfunction of the device etc.

For power reduction BIST is specifically proposed to keep power under the threshold. The test power can be reduced by preventing the transition of data at memory elements during scan shift[10]. Test patterns generated by LFSR can be masked by a test vector inhibiting scheme as not all produced lengthy vectors detect faults. So such tests are eliminated to reduce switching activity with no impact on fault coverage. [8]

A new dimension to power aware BIST was added by low transition test pattern generators. For example, a device in consists of LFSR to feed scan chains through biasing logic and T-type flip flops. These flip flops hold the previous values until their input is asserted, the same value is scanned repeatedly until the output of biasing logic becomes 1[9]. The combination of low transition generator with three weighted pseudorandom pattern generator also reduces BIST switching activity.

The BIST power consumption easily exceeds maximum rating when tested at speed, scan patterns are shifted at a programmable low speed, but only last few cycles and the capture cycle are applied at the maximum frequency. LP test compression schemes adapt to LFSR reseeding to reduce number of transitions by reducing scan-in transitions as the low fill rates deliver identical test data scan chains.

The number of transitions at the input of CUT is reduced by 25% by using bit-swapping LFSR as presented in [2]. This BS-LFSR is found to be capable of optimising power up to 63% during test. So after going through these possibilities here in our project we have integrated BS-LFSR in [2] with the Fully operating PRESTO generator which is designed from the basic architecture of PRESTO in [1].As the switching activity is controlled by toggle selection (TOSE) technique , by embedding bit swapping concept power is further optimised at a far better level.

PROJECT DESCRIPTION

Generally to test any circuit, test patterns are generated and are fed to the circuit-under-test. Here also we generate pseudorandom test patterns by using a linear feedback shift register and are applied to the circuit of interest. The nature of the test vector generator directly influences the tests pattern to fault coverage ratio. So, it is very important to choose apt test pattern generator. In most of the cases, LFSR is used as a pattern generator and we have also chosen it here. Test vectors produced by LFSR are directly not applied to CUT. They are processed or modified accordingly, so that non - repetitive patterns are being fed to test CUT for least possible switching activity. The necessity of the proper choice of an LFSR is shown here, by designing a BIST for the ISCAS benchmarks as the complexity of VLSI circuits is constantly increasing, so there is a need to use built-in self-test (BIST).Hence for more power optimization we use Bit Swapping LFSR here. Built-in self-test enables the chip to test itself and evaluate the response of circuit. Thus, the very complex and expensive external ATE (Automatic Test Equipment) can be omitted completely and its complexity can be significantly reduced.

A. BASIC ARCHITECTURE

The basic architecture of a preselected toggling generator consists of an n-bit PRPG feeding scan chains connected with a phase shifter forms a kernel of the generator producing the pseudorandom test patterns. A linear feedback shift register or a ring generator can used to implement a PRPG. And n hold latches are placed between the PRPG

that is LFSR and the phase shifter. Each hold latch is individually controlled with the corresponding stage of an n-bit toggle control register.

As long as its enable input is high, the latch enters into toggle mode and it is transparent for data fed from PRPG to the phase shifter. When the latch is disabled or low, it captures and saves, the corresponding bit of PRPG for a number of clock cycle feeding the phase shifter and the same scan chains with a constant value. It will now be in the hold mode. XORed outputs of three different hold latches are given to the phase shifter and the output is NOTed. Therefore, all scan chains remain in low-power mode only when disabled hold latches drive the corresponding phase shifter output the toggle control register controls the hold latches. It comprises of 0s and 1s, where 1 indicate latch is in the toggle mode then transparent for data arriving from the PRPG. Their fractions determine the scan switching activity.

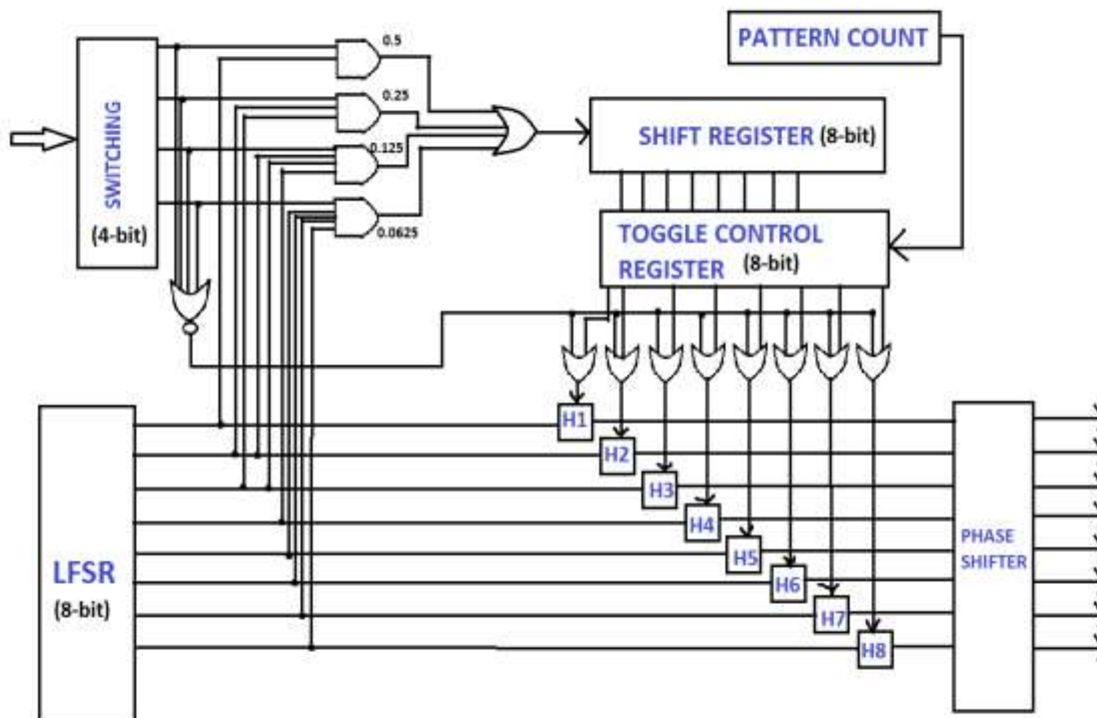

Fig 1: Basic architecture of a PRESTO generator.

Here we use 8-bit LFSR with shift register and toggle control register. The switching will be fed with a 4-bit input.The control register is loaded once per pattern with the data of an additional shift register. The enable signals inserted into the shift register are produced in a probabilistic fashion by using the original PRPG with a set of weights that can be programmed. The weights are determined by one among four AND gates produce 1s with probabilities 0.5, 0.25, 0.125, and 0.0625, respectively. The OR gate allow choosing probability above powers of 2. A 4-bit switching register is employed to activate AND gates, and allow us to select user-defined level of switching activity. If the phase shifter structure is known then the expected toggling ratio is achieved.

When the switching input is given as 0110, then the LFSR out will be a 8-bit data 11100010. Four AND gates will emit 0100 respectively. That means second AND gate is triggered and only 25% of hold latches will be activated as its probability is 0.25, remaining will be disabled. Among eight hold latches H1 will be active and other are not. By XORing the outputs of laches properly, the phase shifter output will be for given data 11000000. Additional 4-input NOR gate at switching register detects the switching input 0000, which is used to switch off the Low power functionality of the generator. It is worth noting when it is working in the weighted random mode; the switching level selector maintains statistically stable content of the control register that is the amount of 1s carried. This results the same fraction of scan chains to stay in the LP mode, though a set of actual low toggling

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chains keep changing from one test pattern to another. It corresponds to the certain level of toggling in those scan chains. The available toggling granularity renders this solution not suitable as it is too rough.

B. ARCHITECTURE OF MODIFIED LFSR

Below figure shows the implementation of general architecture of Bit Swapping LFSR, which reduces the average and weighted switching activity during test operation that reduces number of transitions. Design of Bit Swapping LFSR is based on the captions which are used to describe the Transition activity in Bit Swapping LFSR. We can easily define the process of switching and transition of bits that take place in pattern generation. This description will give surprisingly good results in order to optimize power. For the test-per clock and test-per-scan we have different lemmas. There are several techniques to reduced power consumption.

There is direct technique, if we used reduced frequency during testing it will reduced power dissipation. In this direct technique there is no requirement of extra hardware. Second direct technique to reduced power consumption is to apply appropriate testing planning by doing portioning of CUT into block. These direct techniques increase the timing of testing and are not applicable for reduction peak power. In contrast to the other techniques Bit-Swapping LFSR reduce average and peak power dissipated by CUT. Here we have used 8-bit BS-LFSR which consists of eight D flip-flops, two MUX's and an XOR gate.

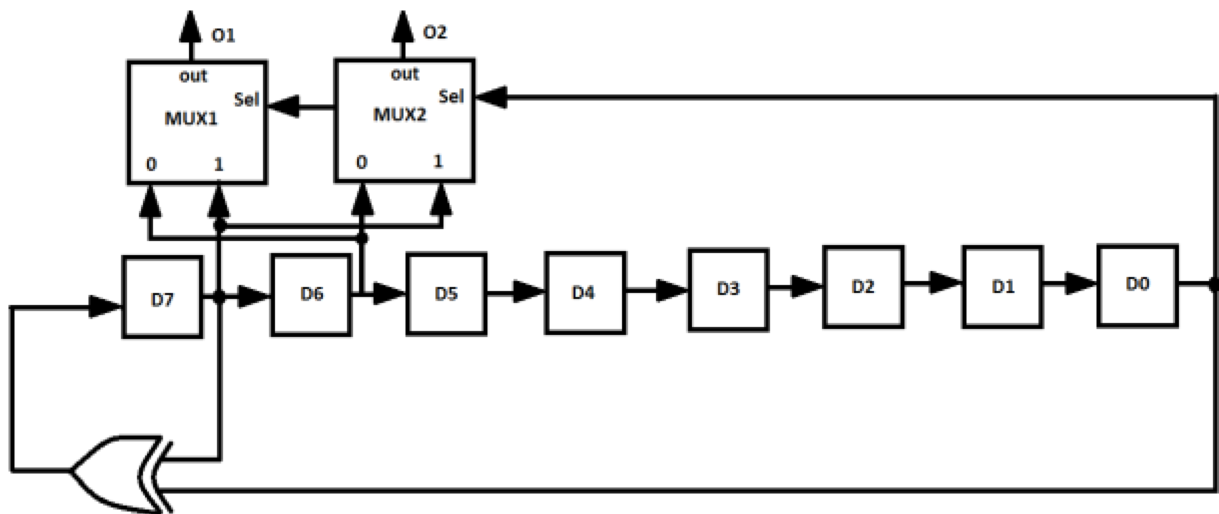

Fig 2. Architecture of bit swapping LFSR

Observation of BS-LFSR: Bit-Swapping LFSR is based on some observations depending upon number of transition produced by LFSR at the output. In modified form of normal LFSR; we have used swapping property between every pair of adjacent cells of normal LFSR for designing Bit-Swapping LFSR. General observation for LFSR, For any n-bit maximum length LFSR that starts with any seed and runs for 2n clock cycles until it returns to the starting seed value, then the total number of transitions T total that occurs is given by the equation T total = n × 2 (n-1).For swapping Bits in BS-LFSR ; If we take any n-bit maximal length LFSR where n is greater than 2 and LFSR is modified with swapping arrangement, we consider one of its outputs 0th i.e. first bit is the selection line that will swap two neighboring bits elsewhere in the LFSR at specific value of selection line. If we set the value of selection line at n for swapping then 0th is odd and bit n =0, bit 7 will be swapped with bit 6, bit 6 with bit 5…bit n-1 with bit n-2. In all cases the selection line has no effect on swapping operation. If bit n =1, then no swapping is performed. In this case, Modified LFSR will be generate exactly same as normal (unmodified) LFSR whereas the order of generated test pattern by modified LFSR will be different. Swapping arrangement will save a number of transitions, swapped bits will save number of transition equal to T Saved = 2(n-2). In contrast, general observation two bits (un-swapped bits) originally produced 2 x 2(n-1) so after swapping the swap bit will therefore save TSaved= 2(n-2)/ (2x 2(n-1) =25%.

PROPOSED TOSE GENERATOR WITH BS-LFSR

For the generation of more flexible test patterns we add few blocks to the basic architecture of TOSE generator so that less toggling and low power consumption is achieved. By preserving the operational principles of the basic

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architecture, proposed architecture uses bit swapping linear feedback shift register and splits up the shifting period of each and every test pattern into a sequence of alternating hold and toggle intervals. To operate the generator back and forth between the two states, a T-type flip-flop is used that switches when there is 1 on its data input. If T-flip flop is set to 0, the generator enters into hold mode with all latches temporarily disabled irrespective of the content of control register. This can be achieved by placing AND gates onto the control register outputs to freeze all phase shifter inputs. This property is critical in System on Chip design where only a single scan chain crosses a given core, and its abnormal toggling will cause unacceptable heat dissipation locally that is only reduced by temporary hold periods.

If the T flip-flop is in the toggle period, then the enabled latches will be able to pass test data through control register from the PRPG to the scan chains. Two additional 4-bit Hold and Toggle registers are used to determine how long the generator remains either in the hold mode or in the toggle mode, respectively. For terminating either mode, the T flip-flop input should be 1. Then weighted pseudorandom signals are produced in a similar fashion to the weighted logic which is used to feed the shift register.

Four 2-input multiplexers routing data from the Toggle and Hold registers are also controlled by T-flip flop. It allows the user to select a source to control data that can be used in the next cycle for changing the operational mode of the generator .For example, when it is in the toggle mode, the input multiplexers observe the Toggle control register (TCR) if the weighted logic output is 1, then flip-flop toggles as a result all hold latches freeze in the previous state. They will remain in this state until the weighted logic output will change to 1. The random occurrence of this event is related to the content of the Hold register that determines when to terminate the hold mode.

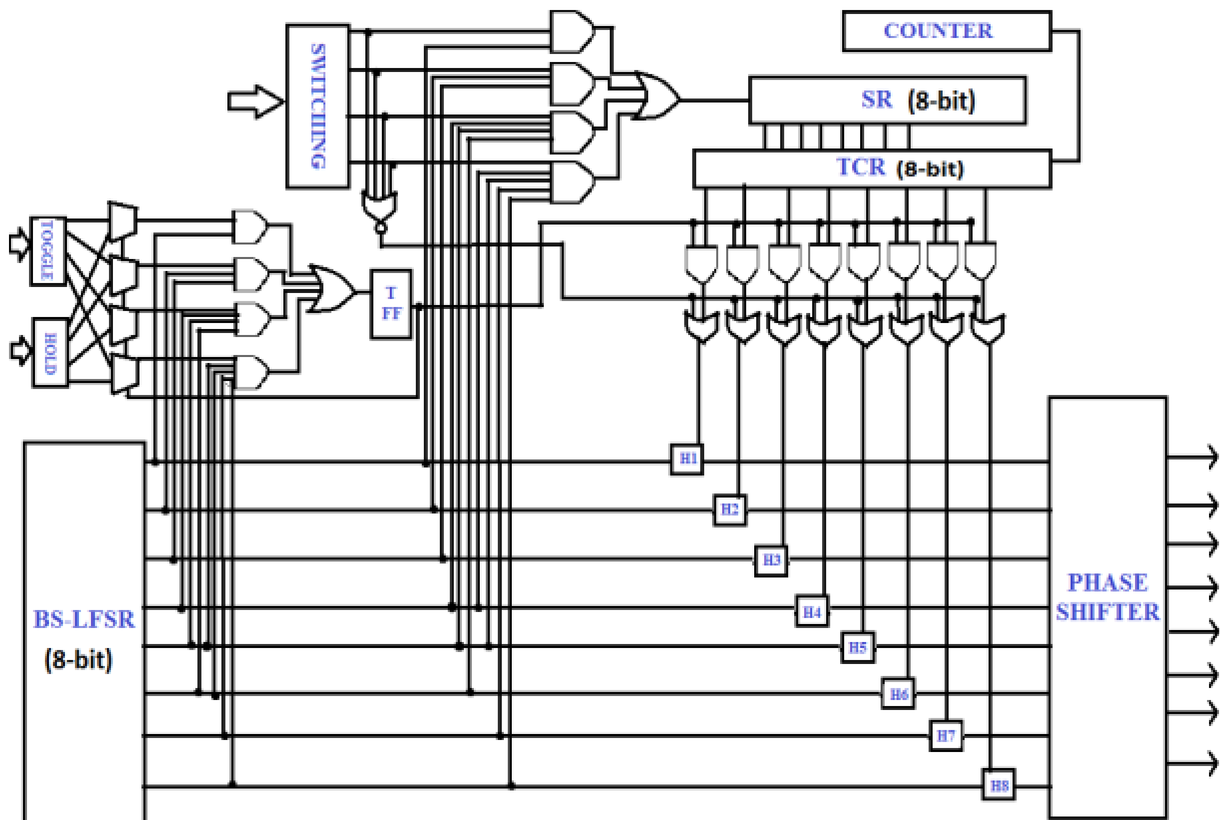

Fig 3. Architecture of TOSE Generator using BS-LFSR.

This fully operational version of the TOSE generator using BS-LFSR reduces power consumption with less switching activity and enhanced fault coverage.

In the next section too test circuits; we have used standard benchmark circuits as circuit under test. ISACS benchmark circuits are used for the analysis of fault coverage and power consumption The ISCAS'89 benchmarks are a set of 31 digital sequential circuits. These benchmark circuits were distributed on tape to participants of the Special Session on Sequential Test Generation. Among 31 circuits we took three s27, s208 and s298. "s" denotes synchronous sequential circuit and the number represent the number of incorrect lines in the circuit primitives.s208 is a frequency divider circuit with 11 primary inputs and 2 primary outputs . Whereas s298 is a traffic light controller circuit with3 inputs, 6 outputs and 133 gates.

RESULTS

Basic_Arch: When inputs are clk= clk ,rst=1 and switch_ip=0110,after it is run for once or twice ,the reset value should be forced to rst=0 . Then the LFSR generates the pattern lfsr_op=10111111 which is fed to the phase shifter based on the activity of hold latches in the path. The TCR and shift register produce tog_op=00000010 and shf_op=00000001 respectively. The phase shifter xor's the inputs from the latches and finally gives the output as ph_shf_op=00000111. The output waveform is shown in the Fig.4

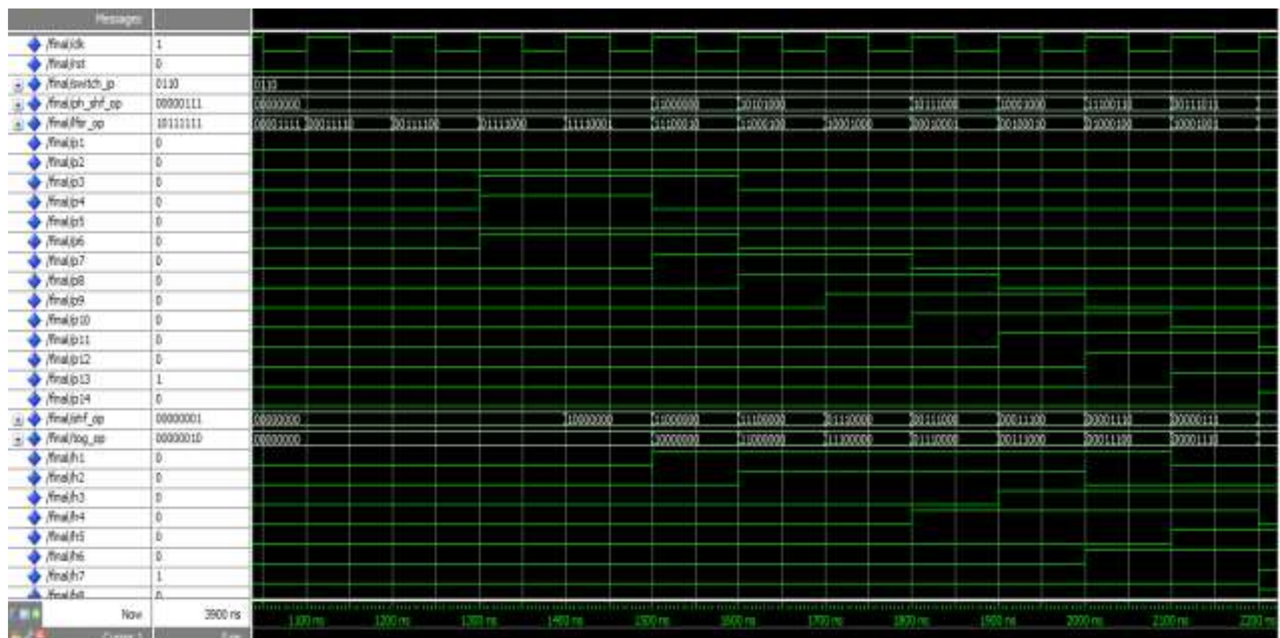

Fig 4: Simulation results of Basic Architecture of existing model

Existing on s27: When inputs are clk= clk ,rst=1 and switch_ip=0010,after it is run for once or twice ,the reset value should be forced to rst=0 . Then the LFSR generates the pattern lfsr_op=10101010 which is fed to the phase shifter based on the activity of hold latches in the path. The TCR and shift register produce tog_op=00000000 and shf_op=00000000 respectively. The phase shifter xor's the inputs from the latches and gives the output as ph_shf_op=00000000. This output vector is fed to the s27 benchmark circuit.For the non-faulty s27 benchmark the output is generated as s_op1=100.We have induced a fault at a node in s27 circuit to test the working of basic architecture, then s_op2=001 is obtained as output. The output waveform is shown in the Fig.5

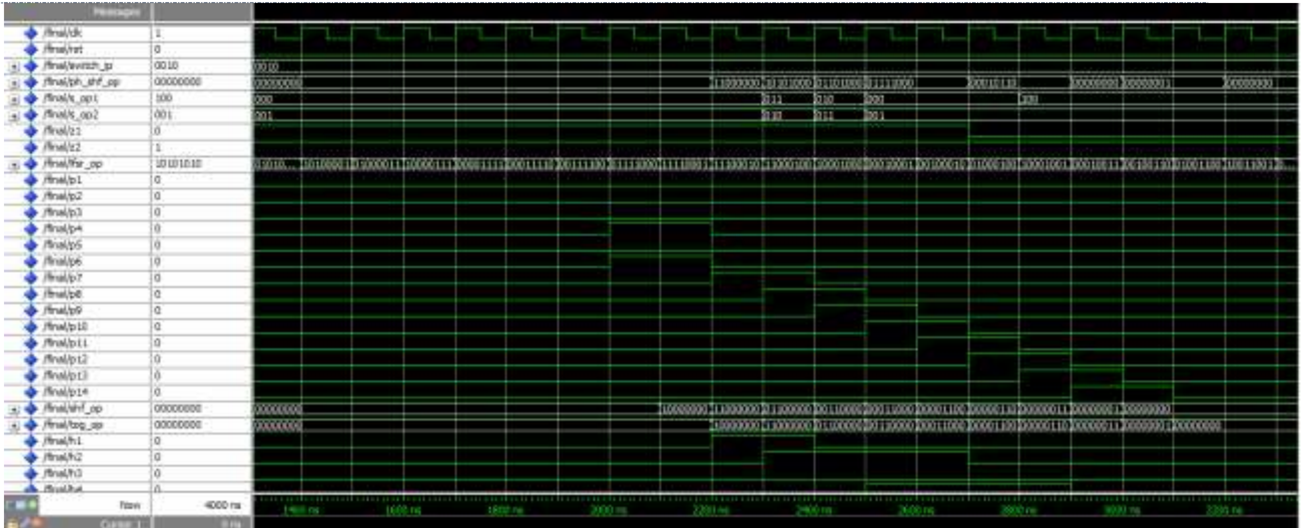

Fig 5: Simulation results of existing model tested over s27 benchmark circuit

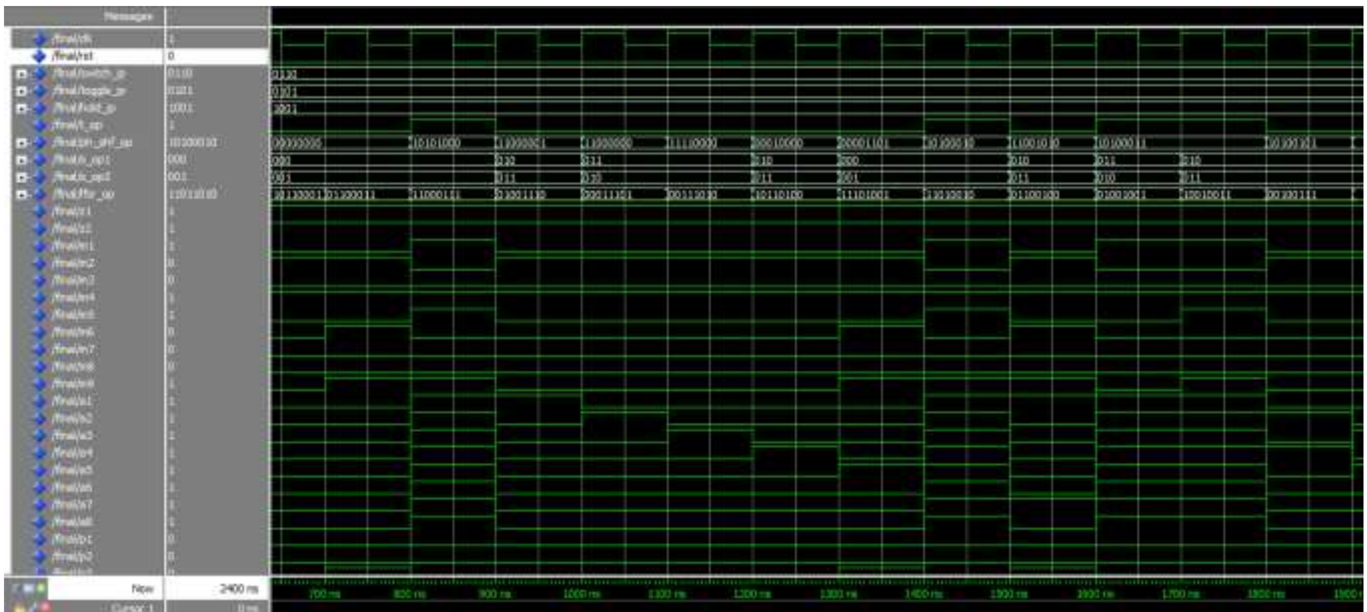

Fig 6: Simulation results of proposed architecture with BS-LFSR tested over s27 benchmark circuit

Proposed Arch with BS-LFSR On s27: When inputs are clk= clk ,rst=1,switch_ip=0110,toggle_ip=0101 and hold_ip=1001,after it is run for once or twice ,the reset value should be forced to rst=0 . Then the LFSR generates the pattern lfsr_op=11011010 which is fed to the phase shifter based on the activity of hold latches in the path.The phase shifter xor's the inputs from the latches and gives the output as ph_shf_op=10100010. This output vector is fed to the s27 benchmark circuit.For the non-faulty s27 benchmark the output is generated as s_op1=000.We have induced a fault at a node in s27 circuit to test the working of basic architecture, then s_op2=001 is obtained as output. The output waveform is shown in the Fig.6.Here we can observe the bit swapping lfsr generates patterns with only one bit change between every adjacent pattern so due to this switching activity of the circuit becomes less as compared to the normal LFSR pattern generation in the random fashion. Hence, this will reduce power consumption of the entire circuit.

The efficiency of our work is analysed used s27,s208 and s298 benchmark circuit of ISACS'89 family. Modelsim and Xilinx are the tools used for simulation and interpretation.

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Design and Power summary Reports:

For Normal LFSR:

S27-EXIS Project Status			
Project File:	s27-exis.ise	**Current State:**	Placed and Routed
Module Name:	final	• **Errors:**	No Errors
Target Device:	xc2s600e-6fg676	• **Warnings:**	4 Warnings
Product Version:	ISE 8.1i	• **Updated:**	Wed Jun 29 15:33:09 2016

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Total Number Slice Registers	31	13,824	1%	
Number used as Flip Flops	23			
Number used as Latches	8			
Number of 4 input LUTs	45	13,824	1%	
Logic Distribution				
Number of occupied Slices	33	6,912	1%	
Number of Slices containing only related logic	33	33	100%	
Number of Slices containing unrelated logic	0	33	0%	
Total Number of 4 input LUTs	45	13,824	1%	
Number of bonded IOBs	45	510	8%	
Number of GCLKs	1	4	25%	
Number of GCLKIOBs	1	4	25%	
Total equivalent gate count for design	494			
Additional JTAG gate count for IOBs	2,208			

Performance Summary

```
Started : "Launching Design Summary".
```

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		139
Vccint 1.80V:	74	133
Vcco33 3.30V:	2	7
Clocks:	50	90
Inputs:	8	15
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Thermal summary:	
Estimated junction temperature:	27C
Ambient temp:	25C
Case temp:	27C
Theta J-A:	17C/W

Invalid Program Mode

Decoupling Network Summary:	Cap Range (uF)	#

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For Proposed method with BS-LFSR:

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Comparision of Results:

Table 1:Comparision of Power dissipation,Delay and Gate Count for S27 Benchmarck Circuit

For S27 Benchmark circuit	Power(mW)	Delay(ns)	Gate Count
Existing architecture with LFSR	139	8.040	494
Modified architecture with BS LFSR	123	6.175	132

Table 2:Comparision of Power dissipation,Delay and Gate Count for S208 Benchmarck Circui

For S208 Benchmark circuit	Power(mW)	Delay(ns)	Gate Count
Existing architecture with LFSR	146	8.270	774
Modified architecture with BS LFSR	126	6.598	189

Table 3:Comparision of Power dissipation,Delay and Gate Count for S298 Benchmarck Circuit

For S298 Benchmark circuit	Power(mW)	Delay(ns)	Gate Count
Existing architecture with LFSR	170	8.578	1018
Modified architecture with BS LFSR	149	8.116	767s

The power consumption and gate count that is area are optimised in the proposed model when compared with the existing architecture.

We have performed testing for three benchmarks namely s27 ,s208 and s298 in all the cases power consumption is reduced.

CONCLUSION AND FUTURESCOPE

The proposed approach aims at the concept reduced switching activity and toggling to reduce power consumption using bit swapping technique in LFSR. It is achieved by generation of non recursive test patterns by choosing proper architecture of the PRPG. The basic architecture is added with additional blocks to achieve granularity in the toggling ratio. PRPG consumes less power during testing by taking the benchmark circuit S27. In the future, power Investigation of LFSRS, Random memory access test and System on chip (soc) memory test can be implemented reduced by modifying internal architecture with reduced complexity. The simulation results show the generated pattern for the applied seed vector. This paper presents the implementation with regard to VHDL language. Synthesizing and implementation of source code is carried out on Xilinx - Project Navigator, ISE 12.3i suite. The power reports show that the proposed TOSE architecture optimizes power by 15 to 20%.

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